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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,608	12/05/2003	Robert S. Chau	42P14705D	9763

7590 09/19/2006

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,608	CHAU ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-44 and 48-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-44 and 48-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *0706*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 07/12/2006.

Claims 31-44 and 48-63 are active in this application.

Claim(s) 1-30, 45-47, and 64-72 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 07/12/2006. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Withdrawal of Allowability

3. The indicated allowability of claims 31-44 and 48-63 is withdrawn in view of the newly discovered reference(s) to Currie et al. (U.S. Patent No. 5,986,291); and/or to Chau et al. (US 2004/0036126). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 31-44 and 48-63 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,986,291 to Currie et al.

Regarding claim 31, Currie discloses a method of forming a transistor, as shown in figs. 1-7, comprising:

forming a narrow bandgap semiconductor film 62 (fig. 4) on an insulating substrate 50;

forming a gate dielectric layer 55 on said narrow bandgap semiconductor film 62;

forming a gate electrode 57 on said gate dielectric 55; and

forming a pair of said source/drain regions 58/59 adjacent to said narrow bandgap semiconductor film 62; wherein said gate electrode 57 and gate dielectric 55 is formed over a portion of said source/drain regions 58/59 (see figs. 1, 4, and col. 12, lines 28-30, and lines 46-49).

Regarding claim 32,Currier disclose the method wherein said narrow bandgap semiconductor film has a bandgap of less than or equal to 0.7 eV. (The channel 62 comprises InGaAs material, which has energy bandgap of about 0.4 - 1.4ev at room temperature; see the free encyclopedia, from Wikipedia, at http://en.wikipedia.org/wiki/Bandgap)

Regarding claim 33, Currie discloses the method wherein said narrow bandgap semiconductor film is selected from the group consisting of InAs, PdTe and InSb. See col. 2, lines 34-36; col. 6, lines 31-40; col. 10, lines 6-7.

Regarding claim 34, Curie discloses the method wherein said source/drain regions 58/59 are formed from a semiconductor film having a larger bandgap than said narrow bandgap semiconductor film (source/drain regions comprising highly doped Si^{+}; col. 9, lines 60-62).

Regarding claims 35-37, Currie discloses the method comprising all claimed limitations. See col. 9, lines 30-67; col. 13, lines 11-17.

Regarding claim 38, Currie discloses the method wherein said metal film forms a Schottky barrier with said narrow bandgap semiconductor film. See col. 9, lines 55-67, col. 10, line 25 to col. 11, line 13.

Regarding claim 39, Currie discloses the method wherein said metal film is selected from the group consisting of titanium nitride, tantalum nitride and hafnium nitride. See col. 9, lines 30-67; col. 10, line 25 to col. 11, line 13; col. 13, lines 11-17.

Regarding claim 40, Currie disclose the method wherein said gate dielectric layer comprises a high dielectric constant film. See col. 9, lines 41-42.

Regarding claim 41, Currie discloses the method wherein said gate electrode comprises a metal film. See col. 8, lines 41-42.

Regarding claim 42, Currie discloses a method of forming a transistor, as shown in figs. 1-7, comprising:

forming an InSb alloy film on an insulating substrate 50 (col. 2, lines 34-36; col. 6, lines 31-40; col. 10, lines 6-7);

forming a high dielectric constant gate dielectric film 55 (fig. 4) on said InSb alloy film;

forming a metal gate electrode 57 on said gate dielectric layer 55; and

forming a pair of source/drain regions 58/59 on opposite sides of said gate electrode 57 on said insulating substrate 50.

Regarding claim 43, Currie disclose the method wherein said source/drain regions 58/59 are formed from a metal film. See col. 9, lines 30-67; col. 13, lines 11-17.

Regarding claim 44, Currie discloses the method wherein said source/drain regions 58/59 are formed from a semiconductor film with a larger bandgap energy than said InSb alloy film. See col. 9, lines 30-32.

Regarding claim 48, Currie discloses a method of forming a transistor, as shown in figs. 1-7,1 comprising:

forming a narrow bandgap semiconductor film 62 (fig. 4) on an insulating substrate 50;

forming a gate dielectric layer 55 on said narrow bandgap semiconductor film 62;

forming a gate electrode 57 on said gate dielectric layer 55; and

forming a pair of source/drain regions 58/59 adjacent to said narrow bandgap semiconductor film 62; wherein said source/drain regions 58/59 are formed from a semiconductor film having a larger bandgap energy than said narrow bandgap semiconductor film (the source/drain regions are formed by highly doped silicon implantation (col. 9, lines 30-32) while the narrow bandgap film 62 is formed by InGaAs).

Regarding claims 49-51, Currie disclose the method comprises all claimed limitations. See figs. 1, 4, 7, and col. 2, lines 34-36; col. 6, lines 31-40; col. 10, lines 6-7.

Regarding claim 52, Currie discloses a method of forming a transistor, as shown in figs. 1-7, comprising:

forming a narrow bandgap semiconductor film 62 on an insulating substrate 50;

forming a high k gate dielectric layer 55 (col. 9, lines 41-42) on said narrow bandgap semiconductor film 62;

forming a gate electrode 57 on said high k gate dielectric 55; and

forming a pair of source/drain regions 58/59 adjacent to said narrow bandgap semiconductor film 62.

Regarding claims 53-60, Curries discloses the method comprising all claimed limitations. See col. 2, lines 34-36; col. 6, lines 31-40; col. 9, lines 30-67; col. 10, lines 6-7; col. 13, lines 11-17.

Regarding claim 61, Currie discloses the method wherein said source/drain regions 57/58 are formed from semiconductor film with a bandgap energy greater than bandgap energy of narrow semiconductor film (the source/drain regions are formed by highly doped silicon implantation (col. 9, lines 30-32) while the narrow bandgap film 62 is formed by InGaAs (fig. 4, 7)).

Regarding claim 62, Currie discloses the method wherein said source/drain regions 57/58 are formed of a metal film. See col. 9, lines 30-67; col. 10, line 25 to col. 11, line 13; col. 13, lines 11-17.

Regarding claim 63, Currie discloses the method wherein said metal film is selected from the group consisting of platinum (Pf), aluminum (Al), and gold (Au). See col. 9, lines 30-67; col. 10, line 25 to col. 11, line 13; col. 13, lines 11-17.

6. Claims 31-44 and 48-63 provisionally rejected under 35 U.S.C. 102(e) as being anticipated by copending Application Publication No. 2004/0036126 (Chau's "126") which has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the copending application, it would constitute prior art under 35 U.S.C. 102(e), if published under 35 U.S.C. 122(b) or patented. This provisional rejection under 35 U.S.C. 102(e) is based upon a presumption of future publication or patenting of the copending application.

This provisional rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the copending application was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131. This rejection may not be overcome by the filing of a terminal disclaimer. See *In re Bartfeld*, 925 F.2d 1450, 17 USPQ2d 1885 (Fed. Cir. 1991).

Regarding claim 31, Chau's "126" discloses a method of forming a transistor comprising:

forming a narrow bandgap semiconductor film 350 (fig. 3, paras. [0019], [0024]) on an insulating substrate 302 (para. 0018]);

forming a gate dielectric layer 322 on said narrow bandgap semiconductor film 308;

forming a gate electrode 324 on said gate dielectric 322; and

forming a pair of said source/drain regions 330/332 adjacent to said narrow bandgap semiconductor film 350; wherein said gate electrode 324 and gate dielectric 322 is formed over a portion of said source/drain regions (fig. 1; paras. [0019], [0023-0024], [0033]; for example, para. [0023] states that source/drain regions 330/332 can include tip or extension regions, that the profile of the source/drain regions may vary in order to obtain a particular electrical characteristic; these imply that the source/drain regions may be extending under the gate structure to form a narrow or short channel device).

Regarding claim 32, Chau's "126" discloses the method wherein said narrow bandgap semiconductor film 350 comprises InSb (para. [0019]), therefore it has a bandgap of less than or equal to 0.7 eV.

Regarding claim 33, Chau's "126" discloses the method wherein said narrow bandgap semiconductor film 350 is selected from the group consisting of InAs, PdTe and InSb. See para. [0019].

Regarding claim 34, Chau's "126" discloses the method wherein said source/drain regions 330/332 are formed from a semiconductor film having a larger bandgap than said narrow bandgap semiconductor film. See paras. [0023-0024].

Regarding claim 35, Chau's "126" discloses the method wherein said source/drain regions 330/332 are formed from a compound semiconductor. See paras. [0023], [0028].

Regarding claim 36, Chau's "126" discloses the method wherein said semiconductor film of said source/drain regions is selected from the group consisting of InAlSb, InP, GaSb, GaP, and GaAs. See paras. [0023], [0028].

Regarding claims 37-41, Chau's "126" discloses the method comprising all claimed limitations. See paras. [0043-0045], [0050].

Regarding claim 42, Chau's "126" discloses a method of forming a transistor comprising:

forming an InSb alloy film 308/350 (fig. 3, paras. [0019], [0024]) on an insulating substrate 302;

forming a high dielectric constant gate dielectric film 322 (para. [0020]) on said InSb alloy film 308/350;

forming a metal gate electrode 324 (para. [0022]) on said gate dielectric layer 322; and

forming a pair of source/drain regions 330/332 on opposite sides of said gate electrode 324 on said insulating substrate 302.

Regarding claim 43, Chau's "126" discloses the method wherein said source/drain regions are formed from a metal film. See paras. [0023], [0028], [0031].

Regarding claim 44, Chau' s "126" discloses the method wherein said source/drain regions 330/332 are formed from a semiconductor film with a larger bandgap energy than said InSb alloy film. See fig. 1; and paras. [0019], [0023-0024], [0033]; for example, para. [0023] states that source/drain regions 330/332 can include tip or extension regions, that the profile of the source/drain regions may vary in order to obtain a particular electrical characteristic; these imply that the source/drain regions may be extending under the gate structure to form a narrow or short channel device.

Regarding claim 48, Chau's "126" discloses a method of forming a transistor comprising:

forming a narrow bandgap semiconductor film 350 (fig. 3, paras. [0019], [0024]) on an insulating substrate 302 (fig. 3);

forming a gate dielectric layer 322 on said narrow bandgap semiconductor film 350;

forming a gate electrode 324 on said gate dielectric layer 322; and

forming a pair of source/drain regions 330/332 adjacent to said narrow bandgap semiconductor film 350; wherein said source/drain regions 330/332 are formed from a semiconductor film having a larger bandgap energy than said narrow bandgap semiconductor film (fig. 1; paras. [0019], [0023-0024], [0033]; for example, para. [0023] states that source/drain regions 330/332 can include tip or extension regions, that the profile of the source/drain regions may vary in order to obtain a particular electrical characteristic; these imply that the source/drain regions may be extending under the gate structure to form a narrow or short channel device).

Regarding claims 49-51, Chau's "126" discloses the method comprising all claimed limitations. See paras. [0019], [0023-0024], [0028], [0033].

Regarding claim 52, Chau's "126" discloses a method of forming a transistor comprising:

forming a narrow bandgap semiconductor film 350 (fig. 3, paras. [0019], [0024]) on an insulating substrate 302;

forming a high k gate dielectric layer 322 (para. [0020]) on said narrow bandgap semiconductor film 350;

forming a gate electrode 324 on said high k gate dielectric 322; and

forming a pair of source/drain regions 330/332 adjacent to said narrow bandgap semiconductor film 350.

Regarding claims 53-60, Chau's "126" discloses the method comprising all claimed limitations. See paras. [0020], [0041].

Regarding claim 61, Chau's "126" discloses the method wherein said source/drain regions are formed from semiconductor film with a bandgap energy greater than bandgap energy of narrow semiconductor film. (fig. 3, paras. [0019], [0024])

Regarding claim 62, Chau's "126" discloses the method wherein said source/drain regions are formed of a metal film. See paras. [0023-0024], [0031], [0050].

Regarding claim 63, Chau's "126" discloses the method wherein said metal film is selected from the group consisting of platinum (Pf), aluminum (Al), and gold (Au). See paras. [0023-0024], [0031], [0050].

Conclusion

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Primary Examiner

Dao H. Nguyen
Art Unit 2818
September 5, 2006